REMARKS

Forty-four claims are pending in the present Application. Claims 1-44 currently stand rejected. Claims 1, 21, and 43 are amended herein. Reconsideration of the Application in view of the foregoing amendments and the following remarks is respectfully requested.

35 U.S.C. § 103

In paragraph 4 of the Office Action, the Examiner rejects claims 1-44 under 35 U.S.C. § 103 as being unpatentable over U.S. Patent No. 5,613,114 to Anderson et al. (hereafter Anderson) in view of U.S. Patent No. 6,519,265 to Liu et al. (hereafter Liu), and further in view of U.S. Patent No. 6,732,235 to Krivacek (hereafter Krivacek). The Applicants respectfully traverse these rejections for at least the following reasons.

Applicants maintain that the Examiner has failed to make a *prima facie* case of obviousness under 35 U.S.C. § 103(a) which requires that three basic criteria must be met, as set forth in M.P.E.P. §2142:

> "First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations."

The initial burden is therefore on the Examiner to establish a *prima facie* case of

obviousness under 35 U.S.C. § 103(a).

Regarding the Examiner's rejection of independent claims 1, 21, and 43, Applicants respond to the Examiner's §103 rejection as if applied to amended claims 1, 21, and 43 which now recite "*a processor that sequentially executes current processes in a non-idle state while said context control module simultaneously preloads isochronous context data needed for executing subsequent processes,*" which are limitations that are not taught or suggested either by the cited reference, or by the Examiner's citations thereto.

Applicants respectfully traverse the Examiner's assertion that modification of the device of Anderson according to the teachings of Liu and Krivacek would produce the claimed invention. Applicants submit that Anderson in combination with Liu and Krivacek fail to teach a substantial number of the claimed elements of the present invention. Furthermore, Applicants also submit that neither Anderson, Liu, nor Krivacek contain teachings for combining the cited references to produce the Applicants' claimed invention. The Applicants therefore respectfully submit that the obviousness rejections under 35 U.S.C §103 are improper.

With regard to the rejections of claims 1-44, the Examiner concedes that "Anderson did not expressly teach a main context that is configured to support system execution tasks and a context module that controls switching procedures between main context and other concurrent contexts." Applicants concur. The Examiner then points to Liu to purportedly remedy these deficiencies. Applicants respectfully disagree with the Examiner's interpretation of the teachings of Liu.

Liu teaches "a memory configured to store instruction modules, each instruction module corresponding to a context . . . ." Liu further teaches a "control state machine that selects one of the instruction modules for execution." Liu is therefore directed towards modules that store program instructions, and not the "context data" that is recited in claims 1, 21, and 43.

Furthermore, the Examiner concedes that "the combined teachings of Anderson and Liu do not expressly teach a system having a processor that sequentially executes processes while said context control module simultaneously preloads isochronous context data needed for executing subsequent processes." Applicants concur. The Examiner then cites column 8, lines 28-39, of Krivacek to purportedly remedy these deficiencies. Applicants respectfully disagree with the Examiner's interpretation of the teachings of Krivacek.

Krivacek generally teaches a digital signal processing system that utilizes cache memory. In particular, Krivacek discusses a situation where "a cache miss results in 8 instructions being written in the cache before execution resumes." In contrast, Applicants explicitly recite "*a processor that sequentially executes current processes in a non-idle state while said context control module simultaneously preloads isochronous context data . . . .*" Applicants therefore submit that their processor is not "stalled", as disclosed by Krivacek.

In addition, Krivacek discloses a download "to either reduce the cache miss rate . . . or execute efficiently in a small memory system . . . ." (column 8, lines 31-39). In contrast, Applicants explicitly recite preloading "isochronous context data needed for executing subsequent processes." Applicants therefore submit

that the claimed purpose of their invention is not "to either reduce the cache miss rate . . . or execute efficiently in a small memory system . . . ," as disclosed by Krivacek.

For at least the foregoing reasons, Applicants therefore submit that neither Anderson, Liu, nor Krivacek teach "*a processor that sequentially executes current processes in a non-idle state while said context control module simultaneously preloads isochronous context data needed for executing subsequent processes,*" as claimed by Applicants.

With regard to claim 44, "means-plus-function" language is utilized to recite elements and functionality similar to those recited in claims 1 and 21 discussed above. Applicants therefore incorporate those remarks by reference with regard to claim 44. In addition, the Courts have frequently held that "means-plus-function" language, such as that of claim 44, should be construed in light of the Specification. More specifically, means-plus-function claim elements should be *construed to cover the corresponding structure, material or acts described in the specification*, and equivalents thereof. Applicants respectfully submit that, in light of the substantial differences between the cited references and Applicants' invention as disclosed in the Specification, claim 44 is therefore not anticipated or made obvious by the teachings of the cited references.

Regarding the Examiner's rejection of dependent claims 2-20 and 22-42, for at least the reasons that these claims are directly or indirectly dependent from respective independent claims whose limitations are not identically taught or suggested, the limitations of these dependent claims, when viewed through or in

combination with the limitations of the respective independent claims, are also not identically taught or suggested. Applicants therefore respectfully request reconsideration and allowance of dependent claims 2-20 and 22-42, so that these claims may issue in a timely manner.

For at least the foregoing reasons, the Applicants submit that claims 1-44 are not unpatentable under 35 U.S.C. § 103 over Anderson in view of Liu, and that the rejections under 35 U.S.C. § 103 are thus improper. The Applicants therefore respectfully request reconsideration and withdrawal of the rejections of claims 1-44 under 35 U.S.C. § 103.

On page 11 of the Office Action, the Examiner rejects claims 1, 21, and 43-44 under 35 U.S.C. § 103 as being unpatentable over Anderson in view of U.S. Patent No. 5,528,513 to Vaitzblit (hereafter Vaitzblit). The Applicants respectfully traverse these rejections for at least the following reasons.

Applicants maintain that the Examiner has failed to make a *prima facie* case of obviousness under 35 U.S.C. § 103(a). As discussed above, for a valid *prima facie* case of obviousness under 35 U.S.C. § 103(a), the prior art references when combined must teach or suggest all the claim limitations." The initial burden is on the Examiner to establish a *prima facie* case of obviousness under 35 U.S.C. § 103(a).

Regarding the Examiner's rejection of independent claims 1, 21, and 43, Applicants respond to the Examiner's §103 rejection as if applied to amended claims 1, 21, and 43 which now recite "*a processor that sequentially executes*

current processes in a non-idle state while said context control module simultaneously preloads isochronous context data needed for executing subsequent processes," which are limitations that are not taught or suggested either by the cited reference, or by the Examiner's citations thereto.

With regard to the rejections of claims 1, 21, and 43-44, the Examiner concedes that "Anderson does not expressly teach . . . a processor that sequentially executes current processes while said context control module simultaneously preloads isochronous context data needed for executing subsequent processes." Applicants concur. The Examiner then points to Vaitzblit to purportedly remedy these deficiencies. Applicants respectfully disagree with the Examiner's interpretation of the teachings of Vaitzblit.

Vaitzblit teaches a general scheduler for multiple classes of tasks (see column 3, lines 15-55). However, after review of the nearly six full columns cited by the Examiner, Applicants respectfully disagree with the Examiner's interpretation of Vaitzblit. Applicants submit that Vaitzblit nowhere discloses a processor that "*sequentially executes current processes*" while a context control module "*simultaneously preloads isochronous context data*" needed for executing subsequent processes, as recited by Applicants. Applicants request the Examiner to indicate specifically where such teachings may be found in Krivacek, or in the alternative, to reconsider and withdraw the foregoing rejections of claims 1, 21, and 43.

With regard to claim 44, "means-plus-function" language is utilized to recite elements and functionality similar to those recited in claims 1 and 21

discussed above. Applicants therefore incorporate those remarks by reference with regard to claim 44. In addition, the Courts have frequently held that "means-plus-function" language, such as that of claim 44, should be construed in light of the Specification. More specifically, means-plus-function claim elements should be *construed to cover the corresponding structure, material or acts described in the specification*, and equivalents thereof. Applicants respectfully submit that, in light of the substantial differences between the cited references and Applicants' invention as disclosed in the Specification, claim 44 is therefore not anticipated or made obvious by the teachings of the cited references.

For at least the foregoing reasons, the Applicants submit that claims 1, 21, and 43-44 are not unpatentable under 35 U.S.C. § 103 over the cited references, and that the rejections under 35 U.S.C. § 103 are thus improper. The Applicants therefore respectfully request reconsideration and withdrawal of the rejections of claims 1, 21, and 43-44 under 35 U.S.C. § 103.

Summary

Applicants submit that the foregoing amendments and remarks overcome the Examiner's rejections. Because the cited references, or the Examiner's citations thereto, do not teach or suggest the claimed invention, and in light of the differences between the claimed invention and the cited prior art, Applicants therefore submit that the claimed invention is patentable over the cited art, and respectfully request the Examiner to allow claims 1-44 so that the present Application may issue in a timely manner. If there are any questions concerning this Response, the Examiner is invited to contact the Applicants' undersigned representative at the number provided below.

Respectfully submitted,

Date: 3/4/06

By: _____

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